Patent

Attorney Docket No.: Intel 2207/7086
Serial No.: 09/750,150
Assignee: Intel Corporation

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT	:	Stephen J. JOURDAN et al.
SERIAL NO.	:	09/750,150
FILED	:	December 29, 2000
FOR	:	MULTI-MODE NON-BINARY PREDICTOR
GROUP ART UNIT	:	2183
EXAMINER	:	Tonia L. MEONSKE

M/S: APPEAL BRIEFS - PATENTS
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Pilar Rodriguez

RESPONSE TO NON-COMPLIANT APPEAL BRIEF

Dear Sir:

This brief is in furtherance of the Notification of Non-Compliant Appeal Brief dated August 12, 2005.

1. REAL PARTY IN INTEREST

The real party in interest in this matter is Intel Corporation. (Recorded April 23, 2001, Reel/Frame 011787/0531).

The Examiner is hereby authorized to charge the appeal brief fee of **$500.00** and any additional fees which may be necessary for consideration of this paper to Kenyon & Kenyon Deposit Account No. **11-0600**.

Respectfully submitted,

KENYON & KENYON

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Message:

Application No.	:	09/750,150	Confirmation No. 6534
Applicant	:	Stephen J. JOURDAN et al.	
Filed	:	December 29, 2000	
Title	:	MULTI-MODE NON-BINARY PREDICTOR	
TC/A.U.	:	2183	
Examiner	:	Tonia L. MEONSKE	

PAPER(s) ENTITLED: Response to Non-Compliant Appeal Brief 18 pages

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2. RELATED APPEALS AND INTERFERENCES

There are no related appeals.

3. STATUS OF THE CLAIMS

Claims 1-26 are pending in this application. Claims 1-26 were rejected under 35 U.S.C. §102(b). This appeal is an appeal from the rejection of claims 1-26.

4. STATUS OF AMENDMENTS

Applicants did not make any amendments to the claim subsequent to final rejection. The claims listed on page 1 of the Appendix attached to this Appeal Brief reflect the present status of the claims (including amendments entered after final rejection).

5. SUMMARY OF THE CLAIMED SUBJECT MATTER

The embodiment of independent claim 1 of the present invention generally describes a method for predicting values in a processor (e.g, Fig.1 - 100, see page 5 line 4) having a plurality of prediction modes, comprising: receiving an instruction at a first table (e.g., Fig. 1 - 122, see page 5 line 24); generating a valid signal (e.g., Fig. 1 - 126, see page 5, line 26) from said first table; providing a prediction mode for said instruction; determining a hit (e.g., Fig. 1 - 126, see page 5, line 26) in a second table (e.g., Fig. 1 - 124, see page 5, line 25), said second table to provide a prediction value (e.g., Fig. 1 - 128, see page 5, line 26), said hit in the second table being determined according to a function of said instruction and said first table; and predicting the predicted value according to said hit and said prediction mode.

The embodiment of independent claim 13 of the present invention generally describes a multi-mode predictor in a processor (e.g, Fig. 1 - 100, see page 5, line 4), comprising: a first table (e.g., Fig. 1 - 122, see page 5, line 24) indexed by an instruction pointer (Fig. 2a - 206, see page 6, line 20) and having table entries that includes a mode field (e.g., Fig. 2a - 212, see page 7, line 15) and an information field (e.g., Fig. 2a - 214, see page 7, line 24); a second table (e.g., Fig. 1 - 124, see page 5, line 25) indexed by a function of said instruction pointer and said first table; and a hit condition (e.g., Fig. 1 - 126, see page 5, line 26) in said second table that correlates to a predicted value (e.g., Fig. 1 - 128, see page 5, line 26) of a prediction mode.

The embodiment of independent claim 19 of the present invention generally describes a processor, comprising: a multi-mode predictor comprising a first table (e.g., Fig. 1 - 122, see page 5 line 24); and a second table (e.g., Fig. 1 - 124, see page 5, line 25), wherein said first table includes a plurality of entry fields and said second table includes a plurality of entry fields, and having a plurality of prediction modes; a set of instructions that index said first table to provide a signal (e.g., Fig. 1 - 126, see page 5, line 26); and a set of predicted values for said set of instructions, said set of predicted values stored in said first table and said second table.

The embodiment of independent claim 24 of the present invention generally describes a multimode predictor, comprising: a first table (e.g., Fig. 1 - 122, see page 5 line 24), indexed by an instruction pointer (e.g., Fig. 1 - 206, see page 6, line 20) and having first table entries, each having a mode field (e.g., Fig. 2a - 212, see page 7, line 15) and a first prediction result field; a function unit having an input for instruction pointer data and coupled to said first prediction result fields of the first table entries, and having an output for a calculated pointer (e.g., Fig. 2a - 214, see page 7, line 24); a second table (e.g., Fig. 1 - 124, see page 5, line 25) indexed by the calculated pointer and having second table (e.g., Fig. 1 - 124, see page 5, line 25) entries having

second prediction result fields; and a selector, having a control input coupled to the mode fields and data inputs coupled to the first and second prediction result fields.

Embodiments of the present invention include a multi-mode predictor for a processor having a plurality of prediction modes. The prediction modes are used to predict non-binary values. The processor includes a multi-mode predictor comprising a per-IP ("PIP") table and a next value table. The PIP table includes a plurality of PIP information fields and the next value table includes a plurality of fields. The multi-mode predictor also includes a plurality of prediction modes. The processor includes a set of instructions that index the PIP table to provide a valid signal. The processor also includes a set of predicted values for the set of instructions. The set of predicted values is stored in the PIP table and the next value table. According to a bit/miss condition in the next value table, a predicted value is selected from the PIP table or the next value table.

Fig. 1 is a block diagram of a multi-mode predictor 120 for use in a PROC 100 in accordance with an embodiment of the present invention. Processor 100 may fetch instructions from memory 112 using fetch unit 110. Instructions retrieved from memory 112 by fetch unit 110 are executed in a pipeline fashion within processor pipeline 130. Instructions are decoded to be executed within pipeline 130.

Multi-mode predictor 120 receives instructions from fetch unit 110 to provide predictions, if applicable.

Multi-mode predictor 120 includes a per-IP ("PIP") table 122 and a next value table 124. Tables 122 and 124 are comprised of fields that store prediction values and other information to generate prediction value 128. PIP table 122 may be indexed according to the IP of the instruction received from fetch unit 110. A match result within the PIP table 122

provides a valid signal 126. Valid signal 126 indicates that a prediction may be provided by multi-mode predictor 120. Preferably, valid signal 126 is a "hit" signal that indicates a hit has occurred in PIP table 122. If no valid signal 126, then a miss has occurred, and no prediction will be provided by multi-mode predictor 120.

Next value table 124 may be indexed by PIP table 122 data and the received instruction as a result of valid signal 126. Depending on the information and data, prediction value 128 is provided by either PIP table 122 or next value table 124. The predicted values correlate to the instructions from fetch unit 110 received at multi-mode predictor 120. If an instruction does not correlate to a predicted value, valid signal 126 will not be provided, and a miss condition noted. The predicted value is selected from PIP table 122 or next value table 124 and is provided as predicted value 128.

Fig. 2a depicts a multi-mode predictor 200 in accordance with an embodiment of the present invention.

Multi-mode predictor 200 includes a PIP table 202 and a next value table 204. Next value table 204 may be indexed by a fixed function 220 of per-IP information field 214 from PIP table 202 and a subset of instruction pointer 206.

Tag field 210 includes address information for comparison to an input address, such as instruction pointer 206. A hit within tag field 210 by instruction pointer 206 generates valid signal 216. Valid signal 216 indicates a hit has occurred in PIP table 202 and that a predicted value 23 0 will be provided for the instruction of instruction pointer 206 by predictor 200. A miss within tag field 210 indicates no prediction is to be provided by predictor 200. The source of the prediction value 230 depends on the current mode within mode field 212 of the PIP table

202 for the specific instruction, and on the hit/miss signal 232 of next value table 204. Next value table 204 may be indexed by the output from fixed function 220.

Logic unit 228 receives various inputs to determine predicted value 230. Hit/miss signal 232 is received from tag field 222 in next value table 204. The mode from mode field 212 also is received from PIP table 202. Logic unit 228 receives last value information from per-IP information field 214. Addition unit 226 provides an input to logic unit 228. Addition unit 226 receives last value and stride information from per-IP information field 214. Logic unit 228 also receives the entry from next value field 224. Logic unit 228 then determines predicted value 230 based on the control inputs received. If hit/miss signal 232 indicates a hit within tag field 222 of next value table 204, then predicted value 230 is the respective entry in next value field 224. If hit/miss signal 232 indicates a miss within tag field 222, then predicted value 230 is the respective entry in per-IP information field 214, with additional manipulations according to the mode. If the mode from mode field 212 is stride, then predicted value 230 is the last value and the stride provided by addition unit 226. If the mode is count or shift, then predicted value is the last value provided by per-IP information field 214. Predicted value 230 preferably is a non-binary value.

Fig. 2b depicts a flowchart of operations for providing a prediction from predictor 200 in accordance with an embodiment of the present invention.

Figs. 3a-d describe the operations of predictor 200 in shift mode according to embodiments of the present invention.

Figs. 4a-c depict the operations of predictor 200 in count mode according to embodiments of the present invention.

Figs. 5a-c depict the operations of predictor 200 in stride mode according to embodiments of the present invention.

Fig. 6 depicts a per-IP information field entry 600 in accordance with another embodiment of the present invention.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Are claims 1-26 anticipated under 35 U.S.C. §102(b) by Wang et al., Highly Accurate Data Value Prediction Using Hybrid Predictors (hereinafter "Wang")?

7. ARGUMENT

A. Claims 1-26 - Anticipation under 35 U.S.C. §102(b) by Wang

The previous Office Action asserts that the limitation "...determining a hit in a second table, *said second table to provide a prediction value*, said hit in the second table being determined according to a function of said instruction and said first table..." of claim 1 can be found in Figure 6 and Section 5.2 of Wang. It further states that:

> However, Wang has in fact taught determining a hit in the second table (Page 288, Figure 6, PHT), *said second table to provide a prediction value* (Page 288, Figure 6), said hit in the second table being determined according to a function of said instruction and said first table (Page 288, Figure 6, The instruction will produce a final prediction from either the VHT or the PHT. When the VHT does not make a prediction then the prediction for the instruction comes from the PHT. The VHT provides values to index into the PHT. The hit, or prediction, from the second table, or PHT, is necessarily a function of the instruction and the first table as the values to index into the second table are provided from the first table.). *(emphasis added)*

Section 5.2 of Wang states:

> The second hybrid predictor that we investigate combines a 2-level predictor and a stride-based predictor. Figure 6 shows the block diagram of this hybrid predictor. Compared to the VHT of the 2-level predictor, this hybrid predictor's VHT entry has two additional

> fields-State and Stride. This hybrid predictor works as follows. When a prediction is to be made for an instruction, the appropriate VHT entry is selected, and its Tag field checked as before. In parallel, the Value History Pattern and the State fields are read out for the 2-level predictor and the stride-based predictor. The 2-level predictor makes a prediction *if the maximum count value in the selected PHT entry is greater than the specified threshold value.* If the 2-level predictor makes a prediction, then that value is selected as the hybrid predictor's prediction. If the 2-level predictor does not make a prediction, then the value predicted (if any) by the stride-based predictor is selected" (*emphasis added).*

Applicants respectfully submit that the PHT disclosed in the Wang reference is not the equivalent of the "second table" as recited in independent claim 1. Contrary to the Office Action's assertion, Applicants respectfully submit that the PHT *does not provide* a *prediction value* as is specifically recited in the embodiment of claim 1, but rather is to determine *whether the 2-level predictor is to generate* a predictor value. Wang's description of Figure 6 specifically states: "The *2-level predictor* (not the PHT) makes a prediction *if the maximum count value in the selected PHT entry is greater than the specified threshold value.* This is affirmed by an examination of Figure 6 (page 288 of Wang) which clearly shows the predicted value to be an output of the 2:1 mux, *not* the PHT table. It is clear that the PHT is merely serving the function of a basic comparator that determines whether the 2-level comparator is to make a prediction. The Wang reference only teaches that upon this comparison made by the PHT, the *entire embodiment described, the "2-level predictor",* makes a prediction. However, it *does not* disclose *the PHT itself* providing a prediction value as specifically described in the embodiment of independent claim 1.

The Advisory Action admits important portions of Applicants' arguments. It states "*Applicant is correct that Wang determines whether the two-level prediction value is to generate a predictor value.* However, the result of this determination is in itself a predictor value." Applicants respectfully submit that this cannot be sufficient to form the basis of a 35 U.S.C.

102(b) rejection. The Advisory Action practically admits that the PHT table is utilized to determine whether the two level prediction value is to generate a prediction value, whereas the embodiment of claim 1 clearly recites "...determining a hit in a second table, *said second table to provide a prediction value*, said hit in the second table being determined according to a function of said instruction and said first table...". The PHT table does not provide the prediction value, and it not sufficient to argue that some other element of Wang may provide a prediction value based on the PHT's operation. Applicants respectfully submit that Wang clearly does not disclose each and every limitation disclosed in independent claim 1, and therefore the Wang reference is inadequate to support a 35 U.S.C. 102(b) rejection. Independent claims 13, 19, and 24 contain substantively similar limitations and therefore should be allowed as well. Claims 2-12, 14-18, 20-23 and 25-26 depend from the aforementioned allowable independent claims, and therefore are in condition for allowance as well.

Next, Applicants further submit the cited references do not disclose "...determining a hit in a second table..." as recited in claim 1. The Office Action further states that the *PHT is the 2nd table where a hit is determined* according to a function of said instruction and said first table and the 2:1 MUX predicts a predicted value according to the "hit" and the "state" field. Applicants respectfully dissent. Again, the relevant section of Wang states: "[t]he 2-level predictor makes a prediction *if the maximum count value in the selected PHT entry is greater than the specified threshold value*". Applicants maintain that the PHT is merely serving the function of a basic comparator circuit that determines whether the 2-level comparator is to make a prediction. The comparison of two numbers in does not comprise a "hit" as disclosed in Applicants' invention. Support for this limitation as used herein can be found at line 24 of page 5 of the specification:

> *Tables 122 and 124 are comprised of fields that store prediction values and other information to generate prediction value 128...* A match result within the PIP table 122 provides a valid signal 126... Preferably, valid signal 126 is a "hit" signal that indicates a hit has occurred in PIP table 122... Depending on the information and data, prediction value 128 is provided by either PIP table 122 or next value table 124... *The predicted value is selected from PIP table 122 or next value table 124 and is provided as predicted value 128. (emphasis added)*

According to an embodiment of the present invention, a match result of a prediction value within the second table results in a "hit". It is clear the comparator PHT in Wang is incapable of providing such a "hit" as defined by the present invention.

Since each and every element of independent claim 1 is not taught, suggested or disclosed by the cited reference, the §102(b) rejection is lacking and should be withdrawn. Independent claims 13, 19, and 24 contain substantively similar limitations and therefore should be allowed as well. Claims 2-12, 14-18, 20-23 and 25-26 depend from the aforementioned allowable independent claims, and therefore are in condition for allowance as well.

Appellants therefore respectfully request that the Board of Patent Appeals and Interferences reverse the Examiner's decision rejecting claims 1-26 and direct the Examiner to pass the case to issue.

APPENDIX

(Brief of Appellants David E. Dent et al.
U.S. Patent Application Serial No. 09/750,150)

8. CLAIMS ON APPEAL

1. (Previously Presented) A method for predicting values in a processor having a plurality of prediction modes, comprising:

receiving an instruction at a first table;

generating a valid signal from said first table;

providing a prediction mode for said instruction;

determining a hit in a second table, said second table to provide a prediction value, said hit in the second table being determined according to a function of said instruction and said first table; and

predicting the predicted value according to said hit and said prediction mode.

2. (Original) The method of claim 1, wherein said predicting includes selecting said predicted value from said first table.

3. (Original) The method of claim 1, wherein said predicting includes selecting said predicted value from said second table.

4. (Original) The method of claim 1, wherein said predicting includes selecting said predicted value from said first table or said second table according said hit in said second table.

5. (Original) The method of claim 1, wherein said generating includes matching a first table tag with said instruction.

6. (Original) The method of claim 5, wherein said generating further includes accessing an information field in said first table correlating to said first table tag.

7. (Original) The method of claim 1, further comprising placing said prediction mode in a shift mode.

8. (Original) The method of claim 1, further comprising placing said prediction mode in a count mode.

9. (Original) The method of claim 1, further comprising placing said prediction mode in a stride mode.

10. (Original) The method of claim 1, wherein said providing includes providing said prediction mode from said first table.

11. (Original) The method of claim 1, further comprising transitioning to said prediction mode from a previous prediction mode.

12. (Original) The method of claim 1, further comprising indexing said second table according to said function and a subset of said instruction.

13. (Previously Presented) A multi-mode predictor in a processor, comprising:

a first table indexed by an instruction pointer and having table entries that includes a mode field and an information field;

a second table indexed by a function of said instruction pointer and said first table; and a hit condition in said second table that correlates to a predicted value of a prediction mode.

14. (Original) The multi-mode predictor of claim 13, wherein said prediction mode is a shift mode.

15. (Original) The multi-mode predictor of claim 13, wherein said prediction mode is a count mode.

16. (Original) The multi-mode predictor of claim 13, wherein said prediction mode is a stride mode.

17. (Original) The multi-mode predictor of claim 13, wherein said first table provides said predicted value.

18. (Original) The multi-mode predictor of claim 13, wherein said second table provides said predicted value.

19. (Original) A processor, comprising:

a multi-mode predictor comprising a first table and a second table, wherein said first table includes a plurality of entry fields and said second table includes a plurality of entry fields, and having a plurality of prediction modes;

a set of instructions that index said first table to provide a signal; and

a set of predicted values for said set of instructions, said set of predicted values stored in said first table and said second table.

20. (Original) The processor of claim 19, wherein said multi-mode predictor further comprises a function that indexes said second table according to said set of instructions and said first table entry fields.

21. (Original) The processor of claim 19, wherein said set of predicted values includes a first set of predicted values stored in said first table, and a second set of predicted values stored in said second table.

22. (Original) The processor of claim 21, further comprising a hit condition in said second table that accesses said second set of predicted values.

23. (Original) The processor of claim 21, further comprising a miss condition in said second table that accesses said first set of predicted values.

24. (Original) A multimode predictor, comprising:

a first table, indexed by an instruction pointer and having first table entries, each having a mode field and a first prediction result field;

a function unit having an input for instruction pointer data and coupled to said first prediction result fields of the first table entries, and having an output for a calculated pointer;

a second table indexed by the calculated pointer and having second table entries having second prediction result fields; and

a selector, having a control input coupled to the mode fields and data inputs coupled to the first and second prediction result fields.

25. (Original) The predictor of claim 24, wherein the first prediction result fields comprise a stride sub-field and a last value sub-field.

26. (Original) The predictor of claim 24, wherein the first table generates a signal indicating whether the instruction pointer hit the first table.

9. EVIDENCE APPENDIX

No further evidence has been submitted with this Appeal Brief.

10. RELATED PROCEEDINGS APPENDIX

Per Section 2 above, there are no related proceedings to the present Appeal.